

**The Hardware Simulator** is used for building and testing all the chips discussed in Nand to Tetris projects 1, 2, 3, and 5.

**Files:** Each chip is defined in a separate `chipName.hdl` file. If you access and edit these files using the Nand2Tetris IDE, the most recent versions of the files are autosaved and persisted in your browser memory. For more information about files handling, select the IDE's Settings and read the File System User Guide.

The simulator features three panels: HDL editor, Pins panel, and Test panel.

### **HDL editor**

**To build or edit a chip** (HDL program), select the chip file using the *project* and *chip* menus. This results in three actions: The `chipName.hdl` file is loaded into the editor, the chip's pins are displayed, and the chip's test script is displayed. Any change that you make to the HDL code is autosaved in the file.

**Builtin chips:** Each chip in projects 1, 2, 3 and 5 has a builtin version. The builtin version features the chip's interface, and a builtin implementation which is part of the simulator's software. The builtin version allows experimenting with the chip's logic before implementing it in HDL. To do so, select the *Builtin* toggle in the HDL panel and test the chip using either interactive or script-based simulation (described next).

### **Pins panel**

Displays the names of the chip's input pins, output pins, and internal pins, and their current values. The pin values are computed by the chip logic when the user clicks the *Eval* button, or when an "eval" command is executed in the chip's test script. If a pin's width is more than one bit, a *dec/bin* toggle allows displaying its value in either a decimal or a binary format. To evaluate a chip interactively, change one or more of its input pin values, and click the *Eval* button.

**A chip is said to be *sequential*** if it contains a sequential chip-part, or if one of its chip-parts contains a sequential chip-part. The DFF chip is sequential. Therefore, any chip that uses one or more DFF chips directly or indirectly is sequential. Sequential chips respond to clock cycles. A clock cycle consists of a tick phase, followed by a tock phase.

**The clock and reset buttons** are enabled for sequential chips only. Clicking the *clock* button advances the clock in either one tick or one tock. Clicking the *reset* button resets the clock.

**Chip visualizations:** The builtin versions of some chips have visualizations, which are displayed automatically by the simulator (and can be turned off). The chip visualizations help inspect the chip's operations, and are useful for educational and debugging purposes. For example, the ALU visualization displays the name of the current ALU operation, and the memory chips visualizations display their internal states.

### **Test panel**

The test panel displays the test script supplied for the loaded chip. The "current command", which is highlighted in yellow, is the test script command that will be executed next. To test a chip, use the *step* button (executes the current command), *run* button (executes the entire test script, from the current command onward), or the *reset* button (makes the first command in the script the current command).

The compare file (if one is supplied) and the output file generated by the test script can be displayed by clicking the respective tabs. If the chip simulation fails, the diff table can be used for inspecting the differences between the chip's expected and actual outputs.

The test script can be edited, but it is recommended to start testing the chip using the supplied script. Changes made to the test script (if any) are not saved.

### **Bug / issue reports**

To report a bug or propose an improvement, click the *bug* icon. You will be asked to login to your GitHub account (if you have one).

*[www.nand2tetris.org](http://www.nand2tetris.org)*